

1 CLAIMS

2 1. In a computing device having a processor that generates a first
3 address signal of a first width and one or more peripheral devices that are
4 addressed with a second address signal of a second width that is greater than the
5 first width, wherein the second address signal is produced in the computing device
6 by concatenating an address extension from an address extension register with the
7 first address signal, a method comprising:

8 concurrently executing threads of a plurality of application programs,
9 wherein different ones of the threads indicate one or more address extensions to an
10 operating system;

11 storing the address extensions for use by the operating system;

12 repeatedly switching between execution of the threads; and

13 prior to executing a particular thread, writing the address extension of the
14 base address indicated by the particular thread to the extension register.

15
16 2. A method as recited in claim 1, wherein the address extensions are
17 indicated as a value of the second width.

18
19 3. A method as recited in claim 1, wherein individual address extensions
20 identify address ranges associated with one or more peripheral devices.

21
22 4. A method as recited in claim 1, further comprising calling an
23 operating system device driver from one of the threads, wherein the device driver
24 invokes an initialization function to indicate the one or more base addresses.
25

sub
A1

6002991019 MS1-317US.PAT.APP.DOC

1 8. A method of scheduling multiple execution threads for interleaved
2 execution by a processor, wherein the processor generates a processor address
3 signal, comprising:

4 executing a first execution thread;
5 writing an address extension to an extension register;
6 concatenating the address extension with the processor address signal to
7 create a peripheral address signal used by the first execution thread;
8 storing the address extension in a location other than the extension register;
9 interrupting the first execution thread to execute portions of one or more
10 other execution threads;
11 interrupting the one or more other execution threads to resume execution of
12 the first execution thread;
13 restoring the stored address extension to the extension register before
14 resuming executing of the first execution thread; and
15 resuming execution of the first execution thread.

16
17 9. A method as recited in claim 8, wherein each address extension
18 identifies an address range associated with one or more peripheral devices.

19
20 10. A method as recited in claim 8, further comprising:
21 writing a second address extension associated with the one or more other
22 execution threads to the extension register;
23 concatenating the second address extension with a second processor
24 address signal to create a second peripheral address signal used by the one or more
25 other execution threads; and

Sub
A1

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

14. A multi-tasking operating system as recited in claim 12, wherein each address extension identifies an address range associated with one or more peripheral devices.

15. One or more computer-readable storage media containing a multi-tasking operating system as recited in claim 12.

16. A computing device comprising:
a processor that generates a first address signal having a first width;
one or more peripheral devices that are addressed with a second address signal having a second width that is greater than the first width;
an address extension register that stores an address extension, wherein the address extension is combined with the first address signal to create the second address signal; and
the processor being programmed to record the address extension being used by a first execution thread, to interrupt the first execution thread to execute portions of one or more other execution threads, to restore the recorded address extension to the address extension register after executing said portions of one or more other execution threads, and to resume the first execution thread after restoring the recorded address extension to the address extension register.

17. A computing device as recited in claim 16 wherein each address extension identifies an address range associated with one or more peripheral devices.

Sub
A1

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

18. A computing device as recited in claim 16 wherein the processor is further programmed to record and restore address extension for a plurality of execution threads.

19. A computing device as recited in claim 16 wherein the processor is programmed to perform the following steps upon interrupting the first execution thread to begin execution of the one or more other execution threads:

recording the address extension being used by the one or more other execution threads; and

interrupting the one or more other execution threads to resume the first execution thread.

20. A computing device comprising:

a processor that generates a first address signal having a first width;

one or more peripheral devices that are addressed with a second address signal having a second width that is greater than the first width;

an address extension register that stores an address extension, wherein the address extension is combined with the first address signal to create the second address signal;

a multi-tasking operating system that switches between execution of different application programs;

a plurality of application programs that use different address extensions, wherein execution threads of the application programs register one or more such address extensions with the multi-tasking operating system;

Sub
A1

6602991019 MS1-317US.PAT.APP.DOC

1 wherein the operating system records the registered address extensions and
2 automatically writes an address extension of a particular application program
3 thread to the address extension register before switching to execution of said
4 particular application program thread.

5
6 **21.** A computing device as recited in claim 20, wherein each address
7 extension identifies an address range associated with one or more peripheral
8 devices.

9
10 **22.** A computing device as recited in claim 20, wherein operating
11 system records the registered address extensions in a memory table.

12
13 **23.** A computing device as recited in claim 20, wherein the execution
14 threads of the application programs invoke operating system device drivers, the
15 operating system device drivers registering said one or more address extensions
16 with the multi-tasking operating system.

17
18 **24.** A computer program stored in a storage medium, comprising:
19 instructions for performing read/write operations on a peripheral device,
20 wherein loading an extension register is a predicate to performing said read/write
21 operations; and

22 instructions for providing one or more address extension values to a multi-
23 tasking operating system for use with one or more threads of the computer
24 program, wherein the operating system automatically loads said one or more
25

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

Sub
AI

28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000

28. A computer program as recited in claim 26, further comprising a step of alternately executing more than one execution thread.

29. A computer program as recited in claim 28, further comprising a step of storing more than one address extension value in memory, each value being associated with a particular execution thread.

30. A computer program as recited in claim 28, further comprising:
storing more than one address extension value in memory, each value being associated with a particular execution thread; and
loading the extension register with the value in memory associated with a particular execution thread prior to resuming execution of that execution thread.

31. A computer program as recited in claim 28, further comprising:
storing more than one address extension value in memory, each value being associated with a particular execution thread; and
loading the extension register with the value in memory associated with a particular execution thread prior to resuming execution of that execution thread;
wherein each address extension identifies an address range associated with one or more peripheral devices.

Sub
A1

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25

32. A computer program as recited in claim 28, wherein the computer program executes an operating system device driver from an interruptible execution thread of the program wherein said device driver identifies a peripheral device to be accessed by the execution thread and identifies a value associated with the execution thread.

add
A1